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PGPB,JPAB,EPAB,DWPI,TDBD	(bus\$3 or (sub adj1 bus\$3)) same (bundle\$1 or group\$1 or together or package\$1) same ((data adj1 flow adj1 processor\$1) or (programmable adj1 gate adj1 arrays))	11	<u>L2</u>
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1 Port calling: a transformation for reducing I/O during multi-packag functional partitioning*Vahid, F.*System Synthesis, 1997. Proceedings., Tenth International Symposium on ,
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2 VLSI technology trends*Koetzle, G.*CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic A
in Intelligent Peripherals and their Interconnection Networks', Proceedings. ,
Page(s): 5/58 -5/62[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) **CNF**

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Abstract

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VLSI technology trends

- Koetzle, G.

IBM Lab., Boeblingen, West Germany

*This paper appears in: **CompEuro '89., 'VLSI and Computer Peripherals. V Microelectronic Applications in Intelligent Peripherals and their Interconnected Networks', Proceedings.***

On page(s): 5/58 - 5/62

8-12 May 1989

1989

ISBN: 0-8186-1940-6

Number of Pages: xiv+791

References Cited: 7

INSPEC Accession Number: 3589210

Abstract:

The trends in VLSI and ULSI technologies are outlined, with emphasis on ASIC (application-specification ICs) and gate arrays. The impact of the present evolution of BICMOS technology on VLSI is discussed, especially in light of CMOS at low temperatures. Packaging technology plays major role in VLSI chip technology and is one of the key factors affecting product competitiveness. It is predicted that thin-film packages (preferably on silicon) for economic reasons will probably be the trend of ever-increasing chip size. Brickwall-packaged VLSI chips connected to extremely wide buses to memory chips on the same carrier result in high processing performance at a low cost. Cooled down to liquid-nitrogen temperatures by means of a cold plate, such (multi-) processors on a single substrate can approach the performance range of bipolar systems at a fraction of their cost.

Index Terms:

packaging; VLSI; ULSI technologies; ASICs; gate arrays; BICMOS technology; thin-film packages; application specific integrated circuits; CMOS integrated circuits; VLSI

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L4: Entry 1 of 15

File: USPT

Sep 18, 2001

US-PAT-NO: 6292021

DOCUMENT-IDENTIFIER: US 6292021 B1

TITLE: FPGA structure having main, column and sector reset lines

DATE-ISSUED: September 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Furtek; Frederick C.	Menlo Park	CA		
Mason; Martin T.	San Jose	CA		
Luking; Robert B.	Catonsville	MD		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Atmel Corporation	San Jose	CA			02

APPL-NO: 9/ 650979

DATE FILED: August 29, 2000

PARENT-CASE:

CROSS-REFERENCE TO RELATED APPLICATIONS This is a divisional application of Ser. No. 09/078,409 filed May 13, 1998 which is a divisional application of Ser. No. 08/650,477 filed May 20, 1996, now U.S. Pat. No. 5,894,565, granted Apr. 13, 1999.

INT-CL: [7] H03K 19/177

US-CL-ISSUED: 326/41; 326/38, 326/93

US-CL-CURRENT: 326/41; 326/38, 326/93

FIELD-OF-SEARCH: 326/37-41, 326/93

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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Keiichi Kawana et al., "An Efficient Logic Block Interconnect Architecture for User-Programmable Gate Array", Proceedings of the IEEE 1990 Custom Integrated Circuits Conference, cat. No. 90CH2860-5, pp. 31.3.1-31.3.4 (May 1990).

ART-UNIT: 289

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Le; Don Phu

ATTY-AGENT-FIRM: Schneck; Thomas Protsik; Mark

ABSTRACT:

A field programmable gate array with a matrix of rows and columns of programmable logic cells interconnectable to each other by a network of local and express bus lines and to I/O pads at the perimeter of the logic cell matrix and bus network, is characterized by having a set of reset lines which include main reset lines, column reset lines, and sector reset lines. Each of the main reset lines receives a different reset signal. Each of the column reset lines is associated with a particular column of logic cells of the matrix. Each column reset line is selectively connectable to any one of the main reset lines to receive a selected reset signal. Each of the sector reset lines is connected to a subset of the logic cells in a column. The column reset lines are selective connectable to the logic cells in this respective associated columns by means of the sector reset lines that are connectable to the column reset lines.

3 Claims, 21 Drawing figures

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L4: Entry 3 of 15

File: USPT

Apr 3, 2001

US-PAT-NO: 6211697

DOCUMENT-IDENTIFIER: US 6211697 B1

TITLE: Integrated circuit that includes a field-programmable gate array and a hard gate array having the same underlying structure

DATE-ISSUED: April 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lien; Jung-Cheun	San Jose	CA		
Feng; Sheng	Cupertino	CA		
Sun; Chung-yuan	San Jose	CA		
Huang; Eddy Chieh	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Actel	Sunnyvale	CA			02

APPL-NO: 9/ 318198

DATE FILED: May 25, 1999

INT-CL: [7] H03K 7/38, H03K 19/177

US-CL-ISSUED: 326/41; 326/39

US-CL-CURRENT: 326/41; 326/39

FIELD-OF-SEARCH: 326/38, 326/39, 326/40, 326/41

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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<input type="checkbox"/>	<u>5805496</u>	September 1998	Batson et al.	365/154
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<input type="checkbox"/>	<u>6031391</u>	February 2000	Couts-Martin et al.	326/38

ART-UNIT: 289

PRIMARY-EXAMINER: Mai; Son

ATTY-AGENT-FIRM: McCutchen, Doyle, Brown & Enersen, LLP

ABSTRACT:

An integrated circuit (IC) includes both a field-programmable gate array (FPGA) and a hard array (HA). The FPGA includes a first set of functional groups that each include an underlying logic structure and memory cells for programming the underlying logic structure, a first set of routing buses, and a first set of routing interconnect areas that provide interconnections between the first set of functional groups and the first set of routing buses. The first set of routing interconnect areas includes transistors and memory cells for programming the interconnections. The HA includes a second set of functional groups that is equal in number to the first set of functional groups and that are arranged like the first set of functional groups. Each functional group in the second set of functional groups includes an underlying logic structure that is like the underlying logic structure of the first set of functional groups but which does not include memory cells for programming the underlying logic structure. The HA also includes a second set of routing buses that are arranged like the first set of routing buses and a second set of routing interconnect areas that are arranged like the first set of routing interconnect areas but which do not include transistors and memory cells for programming interconnections.

17 Claims, 21 Drawing figures

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L4: Entry 5 of 15

File: USPT

Sep 12, 2000

US-PAT-NO: 6118707

DOCUMENT-IDENTIFIER: US 6118707 A

TITLE: Method of operating a field programmable memory array with a field programmable gate array

DATE-ISSUED: September 12, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gould; Scott Whitney	Burlington	VT		
Iadanza; Joseph Andrew	Hinesburg	VT		
Keyser, III; Frank Ray	Colchester	VT		
Zittritsch; Terrance John	Williston	VT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
International Business Machines Corporation	Armonk	NY			02	

APPL-NO: 9/ 189750

DATE FILED: November 10, 1998

PARENT-CASE:

RELATED APPLICATION INFORMATION This application relates to the commonly owned, concurrently or previously filed U.S. patent applications is a divisional of earlier copending U.S. patent application Ser. No. 08/575,312, filed Dec. 20, 1995 now U.S. Pat. No. 5,914,906: 1. Docket No. F19-95-138; Ser. No. 08/575,314 filed Dec. 20, 1995, U.S. Pat. No. 5,719,889, issued Feb. 17, 1998, entitled "PROGRAMMABLE PARITY CHECKING AND COMPARISON CIRCUIT;" and 2. Docket No. F19-95-140, Ser. No. 08/575,422 filed Dec. 20, 1995, U.S. Pat. No. 5,802,003, issued Sep. 1, 1998, entitled: "A SYSTEM FOR IMPLEMENTING WRITE, INITIALIZATION, AND RESET IN A MEMORY ARRAY USING A SINGLE CELL WRITE PORT." Each of these Applications is incorporated herein by reference in its entirety.

INT-CL: [7] G11C 7/00

US-CL-ISSUED: 365/189.08; 326/38, 326/39, 365/230.03

US-CL-CURRENT: 365/189.08; 326/38, 326/39, 365/230.03

FIELD-OF-SEARCH: 365/189.08, 365/230.03, 326/37, 326/38, 326/39

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/>	<u>5692147</u>	November 1997	Larsen et al.	326/39 X

ART-UNIT: 288

PRIMARY-EXAMINER: Hoang; Huan

ATTY-AGENT-FIRM: Heslin & Rothenberg, P.C. Townsend, Esq.; Tiffany

ABSTRACT:

A field programmable memory array having a plurality of sub-arrays is provided. Programmable address decoders, programmable hierarchical bit line arrangements, programmable I/O arrangements, among other features, are provided to enable programming of portions of the array into selected modes. The modes may include wide memory, deep memory, FIFO, LIFO, among others. An embodiment of the invention is disclosed wherein the field programmable memory array is integrated with the programmable resources of a field programmable gate array.

2 Claims, 60 Drawing figures

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L2: Entry 7 of 11

File: EPAB

Nov 11, 1997

PUB-NO: US005687325A

DOCUMENT-IDENTIFIER: US 5687325 A

TITLE: Application specific field programmable gate array

PUBN-DATE: November 11, 1997

INVENTOR-INFORMATION:

NAME

COUNTRY

CHANG, WEB

US

INT-CL (IPC): G06F 15/31

ABSTRACT:

An application specific field programmable gate array ("ASFPGA") includes at least two fixed functional units in a single IC chip. Depending upon a specific application for the ASFPGA, the fixed functional units may include one or more bus interfaces, event timers, an interrupt controller, a Direct Memory Access ("DMA") controller, system timers, a real-time clock, a Random Access Memory ("RAM"), a clock synthesizer, a RAM Digital-to-Analog Converter ("DAC"), a display interface, a register file, a compressed image encoder/decoder ("CODEC"), or similar functional units. The ASFPGA also includes a general purpose field programmable gate array ("FPGA"). The FPGA is configurable to effect a specific digital logic circuit interconnection between fixed functional units. After the FPGA has been configured, the fixed functional units together with the FPGA perform all the functions specified for a particular ASIC design.

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L2: Entry 6 of 11

File: EPAB

Jun 2, 1998

PUB-NO: US005761078A

DOCUMENT-IDENTIFIER: US 5761078 A

TITLE: Field programmable gate arrays using semi-hard multicell macros

PUBN-DATE: June 2, 1998

INVENTOR-INFORMATION:

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INT-CL (IPC): G06F 17/50

EUR-CL (EPC): G06F017/50

ABSTRACT:

A computer implemented method for the automated placement and routing in the design of field programmable gate arrays achieves optimal timing. In a library of primitives and macros from which a designer may choose to implement a given circuit design, at least some of said macros are "semi-hard" macros where direct connections and relative placements are specified while local bus routing is requested in a manner that does not restrict macro placement. A logical netlist containing references to macros and how to connect them together to perform a logical function is first created. The logical netlist is then translated to a physical netlist using a mapper function. This physical netlist for the semi-hard macros specifies what is to be connected but not how. The best place to put each macro on the field programmable gate array is found using a placer function. The placer function thus determines an absolute position of the macros. Pre-defined macro direct connections are routed using a router function. The router function determines an optimal path to connect the semi-hard macros. Finally, a bitstream is generated from placement and routing information developed by the placer and router functions to program the field programmable gate array to perform the netlist logical function.

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File: USPT

Aug 28, 2001

US-PAT-NO: 6282627

DOCUMENT-IDENTIFIER: US 6282627 B1

TITLE: Integrated processor and programmable data path chip for reconfigurable computing

DATE-ISSUED: August 28, 2001

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APPL-NO: 9/ 446762

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FIELD-OF-SEARCH: 712/37, 712/11, 712/13, 712/15, 712/20

PRIOR-ART-DISCLOSED:

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ART-UNIT: 273

PRIMARY-EXAMINER: Coleman; Eric

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ABSTRACT:

The present invention, generally speaking, provides a reconfigurable computing solution that offers the flexibility of software development and the performance of dedicated hardware solutions. A reconfigurable processor chip includes a standard processor, blocks of reconfigurable logic (1101, 1103), and interfaces (319a, 319b, 311) between these elements. The chip allows application code to be recompiled into a combination of software and reloadable hardware blocks using corresponding software tools. A mixture of arithmetic cells and logic cells allows for higher effective utilization of silicon than a standard interconnect. More efficient use of configuration stack memory results, since different sections of converted code require different portions of ALU functions and bus interconnect. Many types of interfaces with the embedded processor are provided, allowing for fast interface between standard processor code and configurable "hard-wired" functions.

29 Claims, 30 Drawing figures